#4

Sheet 1 of 1

FORM PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
162.7513USU	10/056,343
Applicant	
Bhattacharya et al.	
Filing Date	**Group Art Unit**
January 24, 2002	~~2823~~ 2825

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, Etc.)

PP	Kazuo Taki, "*A Survey for Pass-Transistor Logic Technologies*", IEEE, 1998, pp. 223-226.
PP	Mineo Kaneko and Jialin Tian, "*Concurrent Cell Generation and Mapping for CMOS Logic Circuits*", IEEE, 1997, pp. 247-259.

EXAMINER	DATE CONSIDERED
Khellaka Kike	11/15/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP §609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.